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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Applicant: Richard X. Gu, et al.

Docket Number: TI-37591

Serial No.: **10/828,676**

Art Unit: 2817

Filed: 4/21/04

Examiner: James E. Goodley

For: Cross Coupled Voltage Controlled Oscillator

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FACSIMILE COVER SHEET

X FACSIMILE COVER SHEET ___ NEW APPLICATION ___ DECLARATION ___ ASSIGNMENT ___ FORMAL DRAWINGS ___ INFORMAL DRAWINGS ___ CONTINUATION APP'N ___ DIVISIONAL APP'N	___ AMENDMENT ___ (# pages) ___ EOT ______ ___ NOTICE OF APPEAL X APPEAL BRIEF & TRANSMITTAL (12 pages) ___ ISSUE FEE & PUBLICATION FEE (1 Page) ___ REPLY BRIEF (# Pages)
NAME OF INVENTOR(S): Richard X. Gu, et al.	RECEIPT DATE & SERIAL NO.: Serial No.: 10/828,676 Filing Date: 4/21/04
TITLE OF INVENTION: Cross Coupled Voltage Controlled Oscillator	
TI FILE NO.: TI-37591 DEPOSIT ACCT. NO.: 20-0668	
FAXED: 4-7-06 DUE: 4-7-06 ATTY/SEC'Y: AKS/kjv	

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Applicant: Richard X. Gu, et al. | **Art Unit: 2817**

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Filed: 04/21/04 | **Docket: TI-37591**

For: CROSS COUPLED VOLTAGE CONTROLLED OSCILLATOR

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Karen Vertz ____ 4-7-06
Karen Vertz ____ Date

Transmitted herewith is an Appeal Brief in the above-identified application. The Commissioner is hereby authorized to charge the ***$500.00*** fee for this appeal, or credit any overpayment to Account No. 20-0668.

Respectfully submitted,

Alan K. Stewart
Registration No. 35,373

Texas Instruments, Incorporated
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Dallas, Texas 75265

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Richard X. Gu, et al. **Art Unit:** 2817

Serial No.: 10/828,676 **Examiner:** James E. Goodley

Filed: 04/21/04 **Docket:** TI-37591

For: CROSS COUPLED VOLTAGE CONTROLLED OSCILLATOR

APPELLANTS' BRIEF UNDER 37 C.F.R. §1.192

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Karen Vertz 4-7-06
Karen Vertz Date

Dear Commissioner:

The following Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed October 12, 2005. Please charge all required fees, including any extension of time fees, to the deposit account of Texas Instruments Incorporated, Deposit Account No. 20-0668.

04/10/2006 RFEKADU1 00000036 200668 10828676
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REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, to whom this application is assigned.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Applicant's legal representative.

STATUS OF THE CLAIMS

Claims 1-11 are the subject of this appeal. Claims 1-11 are rejected. This application was filed on April 21, 2004.

STATUS OF THE AMENDMENTS

The Appellants filed an amendment under 37 C.F.R. § 1.116 on December 16, 2005 in response to the Office Action dated October 12, 2005, with no amendments to the claims.

SUMMARY OF CLAIMED SUBJECT MATTER

The oscillator circuit 10 shown in Figure 1 comprises a plurality of ring oscillators, specifically four ring oscillators. Each ring oscillator comprises three stages. The four, three-stage ring oscillators in the oscillator circuit 10 are (denoted in terms of the reference labels A-H) ABC, EFG, AGH, and ECD. That is, one three-stage ring oscillator comprises cells A, B and C. Another three-stage ring oscillator comprises cells E, F, and G. The other two three-ring oscillators comprise elements A, G, and H and cells E, F, and G. Three-stage ring oscillator ABC is configured so that the output of cell A couples to the input of cell B. The output of cell B couples to the input cell C and the output of cell C loops back and couples to the input of cell A. Similarly, three-stage ring oscillator EFG is configured so that the output of cell E couples to the input of cell F. The output of cell F couples to the input cell G and the output of cell G loops back and couples to the input of cell E. Further still, three-stage ring oscillator AGH is configured so that the output of cell A couples to the input of cell G. The output of cell G couples to the input cell H and the output of cell H loops back and couples to the input of cell A. Finally, the three-stage ring oscillator ECD is configured so that the output of cell E couples to the input of cell C. The output of cell C couples to the input cell D and the output of cell D loops back and couples to the input of cell E.

As noted above, the frequency of oscillation of a ring oscillator is inversely proportional to the number of stages comprising the ring oscillator. Because the ring oscillators in the oscillator circuit 10 comprise only three cells (stages), the ring oscillators are capable of higher oscillation frequencies than if more than three stages are used.

Each ring oscillator produces an oscillatory output signal. The oscillator circuit 10 of Figure 1 preferably produces four output signals, also called clocks. The output clocks comprise the output of cells A, B, E, and F. The four output clocks all have exactly or approximately the same frequency, but differ in phase. The phase difference between the clocks is an integer multiple of 90 degrees. The output of cell A is referred as "CLK0" to indicate 0 degrees. The output of cell B is referred to as "CLK90" to indicate 90 degrees. Similarly, the outputs of cells E and F are referred to as "CLK180" and CLK270" to indicate 180 and 270 degrees, respectively. The preferred oscillator architecture depicted in Figure 1 thus produces a four-phase clock (CLK0, CLK90, CLK180, and CLK270) while using only three-stage ring oscillators. Three-stage ring oscillators permits high speed clocks to be produced, while the architecture of Figure 1 produces a quadrature clock set.

The four, three-stage ring oscillators are cross-coupled as shown in Figure 1. The ABC ring oscillator couples to the ECD ring oscillator. Specifically, the output of cell C in the ABC ring oscillator drives the input of cell D in the ECD ring oscillator. The output of cell G in the EFG ring oscillator drives the input of cell H in the AGH ring oscillator. The output of cell A in the AGH ring oscillator drives the input of cell B in the ABC ring oscillator. Finally, the output of cell E in the ECD ring oscillator drives the input of cell F in the EFG ring oscillator. The four, three-stage ring oscillators are thus cross-coupled in such a way that each ring oscillator drives only one other ring oscillator. Because each ring oscillator drives one and only one other ring oscillator, the loading on each ring oscillator and cell is minimized which further enables the high-speed nature of the oscillator circuit 10.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claim 1 stands rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,870,431.

ARGUMENT

Rejection under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,870,431

Claims 1-11

Claim 1 includes "... wherein the ring oscillators are directly cross coupled such that each ring oscillator drives only one other ring oscillator." Claim 8 includes "...directly cross-coupling the ring oscillators such that each ring oscillator drives one and only one other ring oscillator." U.S. Patent No. 6,870,431 does not show, teach, or suggest the above recited limitations of claims 1 and 8. For example, U.S. Patent No. 6,870,431 does not teach directly cross-coupling the ring oscillators. U.S. Patent No. 6,870,431 has locking circuits L1 and L2 coupled between the ring oscillators. Therefore the ring oscillators in U.S. Patent No. 6,870,431 are not directly cross-coupled.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-11 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

Alan K. Stewart
Attorney for Appellants
Registration No. 35,373

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CLAIMS APPENDIX

1. An oscillator circuit, comprising:

a plurality of ring oscillators,

wherein each ring oscillator produces an oscillatory output signal; and

wherein the ring oscillators are directly cross coupled such that each ring oscillator drives only one other ring oscillator.

2. The oscillator circuit of claim 1 wherein each ring oscillator comprises three stages.

3. The oscillator circuit of claim 2 wherein each stage comprises an inverter or a delay element.

4. The oscillator circuit of claim 1 wherein the oscillator circuit comprises four ring oscillators, each ring oscillator comprising three stages, and wherein the oscillator circuit produces a four phase clock comprising the oscillatory output signals from each of the four ring oscillators.

5. The oscillator circuit of claim 4 wherein the four oscillatory output signals vary in phase by 90 degrees.

6. The oscillator circuit of claim 1 wherein the plurality of ring oscillators comprise a first cell, a second cell, a third cell, a fourth cell, a fifth cell, a sixth cell, a seventh cell and

an eight cell, each cell having an input and an output and wherein the output of the first cell connects to the inputs of the second seventh cells, the output of the second cell connects to the input of the third and fifth cells, the output of the third cell connects to the input of the fourth and first cells, the output of the fourth cell connects to the input of the fifth and eight cells, the output of the fifth cell connects to the input of the sixth cell, the output of the sixth cell connects to the input of the seventh cell, and the output of the seventh cell connects to the inputs of the eight and fifth cells.

7. The oscillator circuit of claim 1 wherein the plurality of ring oscillators implement differential signaling and the oscillator circuit further comprises a plurality of cells coupled to the ring oscillators and whose purpose is to reduce timing differences among at least some of the oscillator output signals.

8. A method, comprising:

providing a plurality of ring oscillators; and

directly cross-coupling the ring oscillators such that each ring oscillator drives one and only one other ring oscillator.

9. The method of claim 8 wherein providing the plurality of ring oscillators comprises providing a plurality of three-stage ring oscillators.

10. The method of claim 9 further comprising providing quadrature clocks.

11. The method of claim 8 wherein providing the plurality of ring oscillators comprises providing four, three-stage ring oscillators.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.